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Float to Fix conversion

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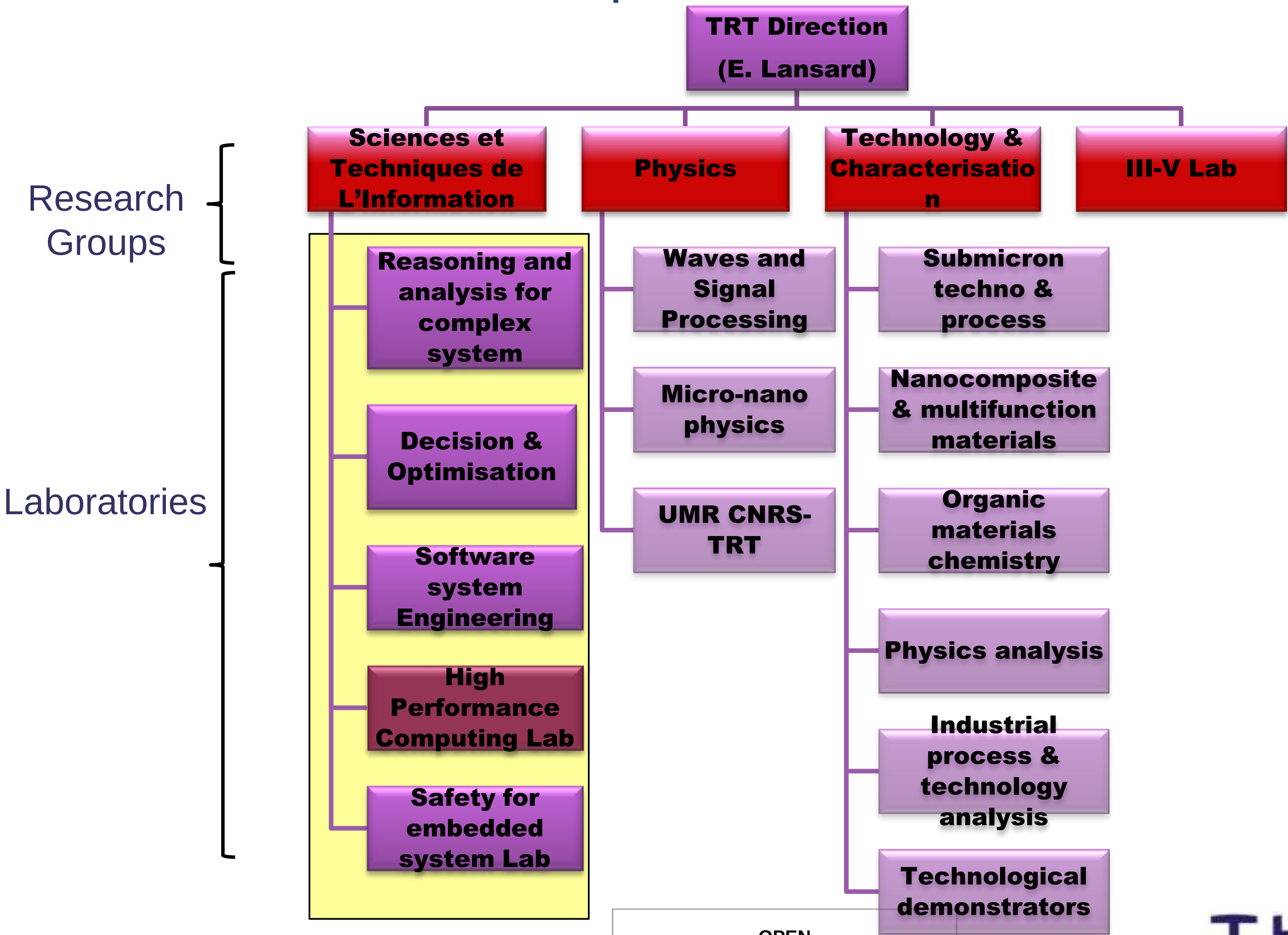
Date /Référence

Thales Research & Technology :

Objective: to propose technological breakthrough for the future products of Thales



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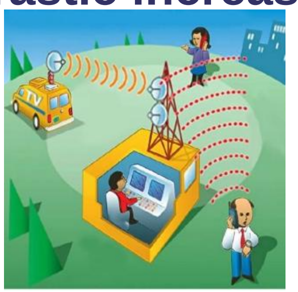
Key issues

Applications

- Algorithms becoming dynamic and irregular, solve the issue of reconfigurable computing.
- Emerging algorithms in sensors raise technical challenges to architectures : beyond Von Neuman, beyond Moore.
- Applications become a mixture of computing levels (data flow, control)
- Drastic increase of data bandwidth out of the sensors



Cognitive radio

Smart camera

Drone

Design methodology

- Improve the link between algorithms and architecture
- Modularity and reuse

Reliability

- Sub-micronic technologies are less and less reliable

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The best trade off to raise the computing power for a low power consumption is obtained through:

- Parallelisation
- Customisation

Australian Desert Animal: the Thorny Devil

In the same time, we have to keep in mind the necessity of flexibility and programming efficiency.

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Why FPGA technology ?

- **High throughput**
- **Low power consumption (no compliant with GPGPU)**

Problem: floating-point computation is not efficient on FPGA (ratio of 5)

The architecture design has to be in fixed-point

BUT: the applications are generally coded in floating-point double precision

The application has to be converted from floating-point to fixed-point: important impact on development flow (TTM, NRC)

Fixed-point Arithmetic: Viewpoint from Industry

Reduce development cost on FPGAs and MPSoC without floating-point unit

- Today this task is done by hand and can cost up to 6 man-months

Avoid reject of designing efficient hardware accelerators on FPGAs

Fixed-point arithmetic brings clear advantages in

- Area, speed, power, communication bandwith

- **Hardcoded IPs**
  - Necessary when volume of data is too important or latency is too short
  - Conversion from floating-point to VHDL representation
- **Dedicated processors**
  - When possible, dedicated processors are better due to programming efficiency
  - Conversion from floating-point to assembly code

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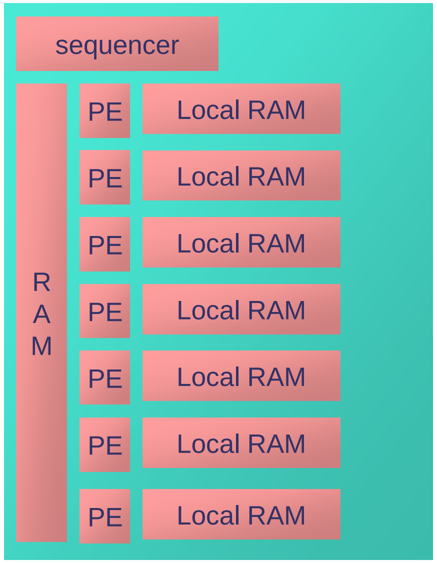
Ter@pix core: an accelerator for Image processing

SIMD :

- The sequencer execute the microcode
- All PEs (based on MULACC operator) execute the same instruction

PE (Processing Element) :

- ALU based on a MULACC
- Local RAM (512 registers)
- 2 lines of the RAM



Accelerator : SIMD

Computing power : 50 Gops on Xilinx Virtex-5 SX240

Consumption : ~15W

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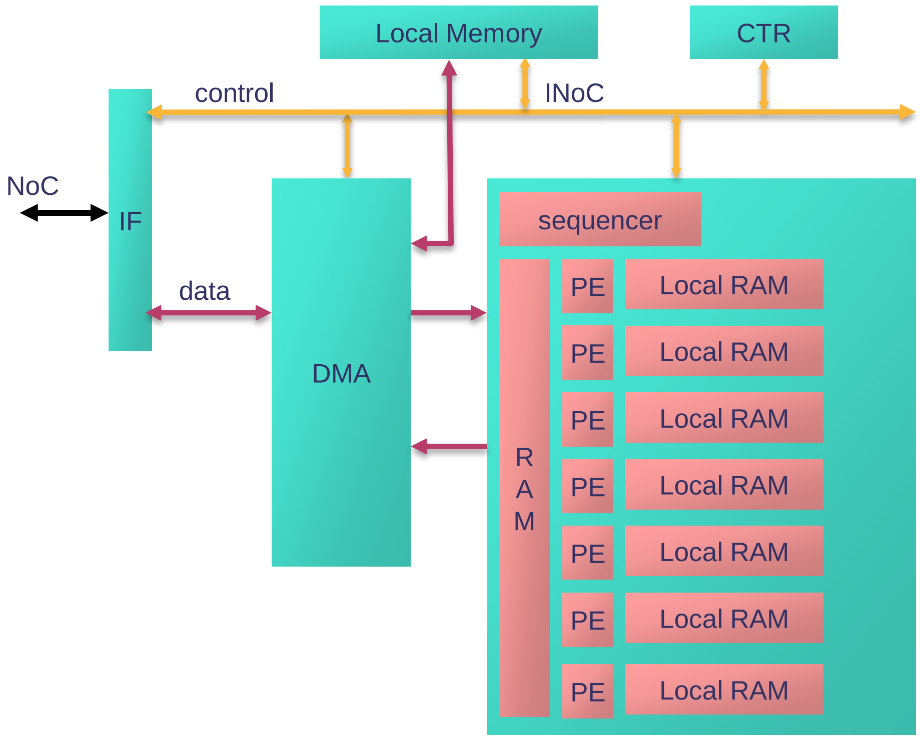
Ter@pix core: an accelerator for Image processing



Accelerator : SIMD

Common functions necessary to use an accelerator :

- DMA to transfer data be computed
- CTR (controler) to execute the correct scheduling between data transfers and works
- Local Memory

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TeraTS: Application domains for Thales Airborne System

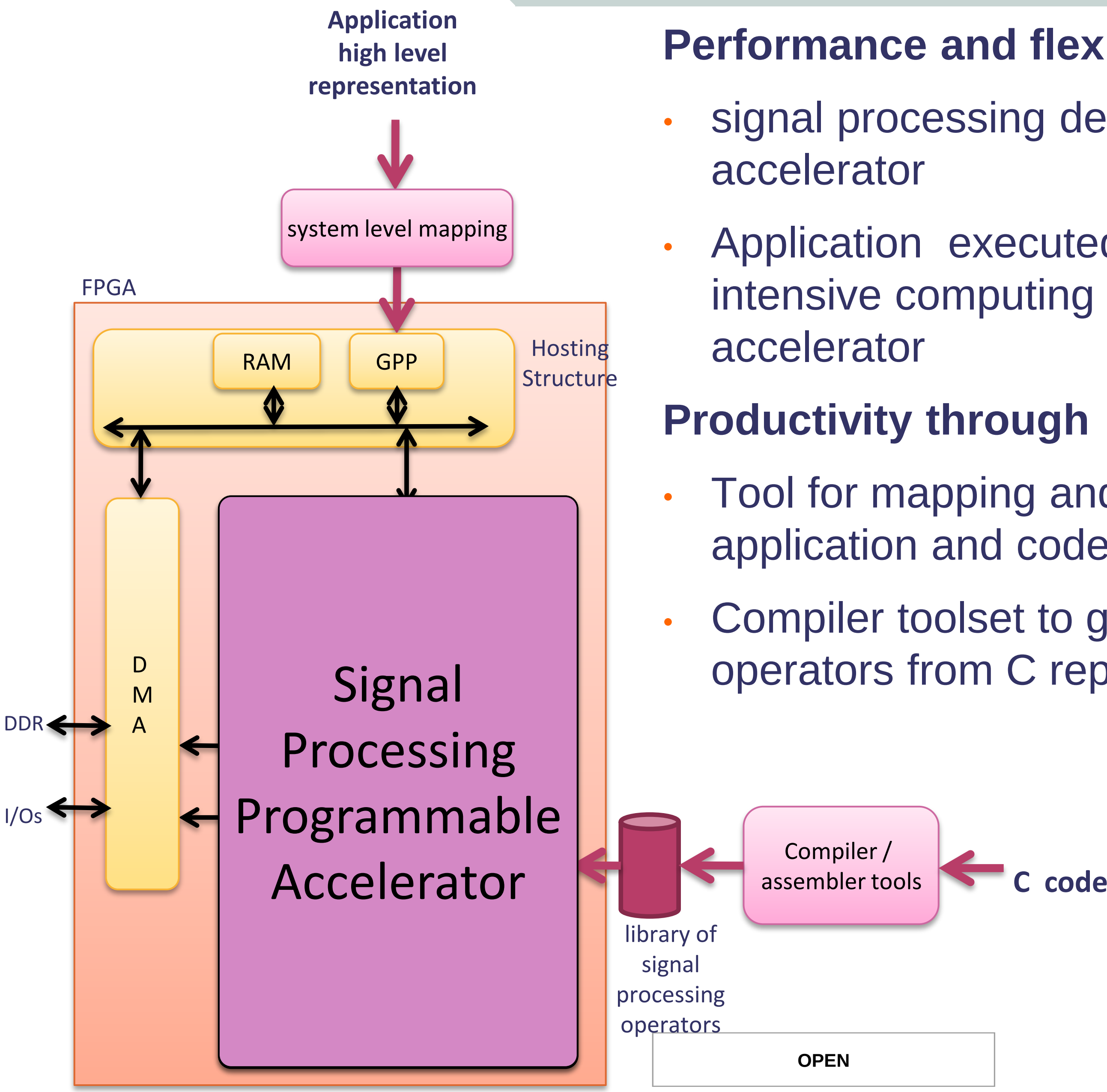
Airborne radar

- **Future requested power computing:**
  - Hundreds of Gops → STAP algorithm (Space Time Adaptive Processing)
- **high volume of data**
  - need of external memory → Issue on bandwidth

Electronic Warfare

- **Future required computing power:**
  - Hundreds of Gops per channel
- **computing directly in the data flow with a short latency : few µs**
- **High frequency**
- **Small array of data**

TeraTS: Solution



Performance and flexibility through

- signal processing dedicated programmable accelerator
- Application executed on a GPP calling intensive computing operators on the accelerator

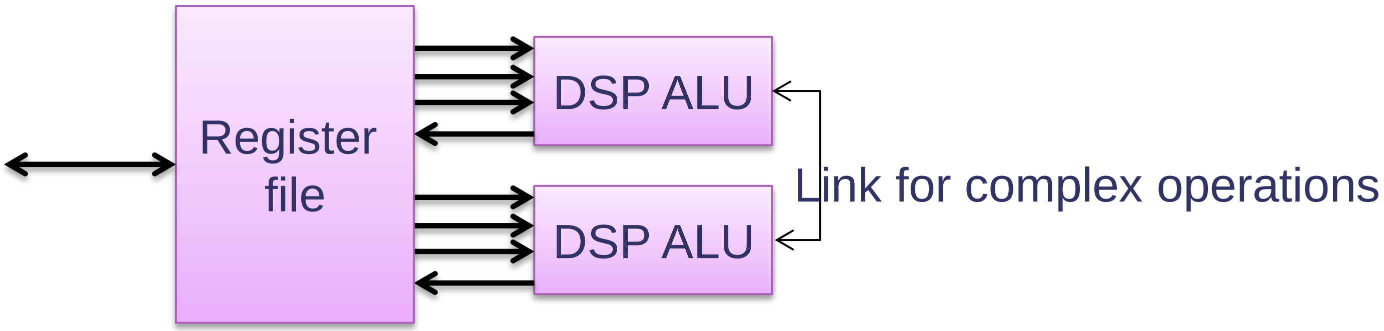
Productivity through

- Tool for mapping and parallelisation of the application and code generation
- Compiler toolset to generate the library of operators from C representation

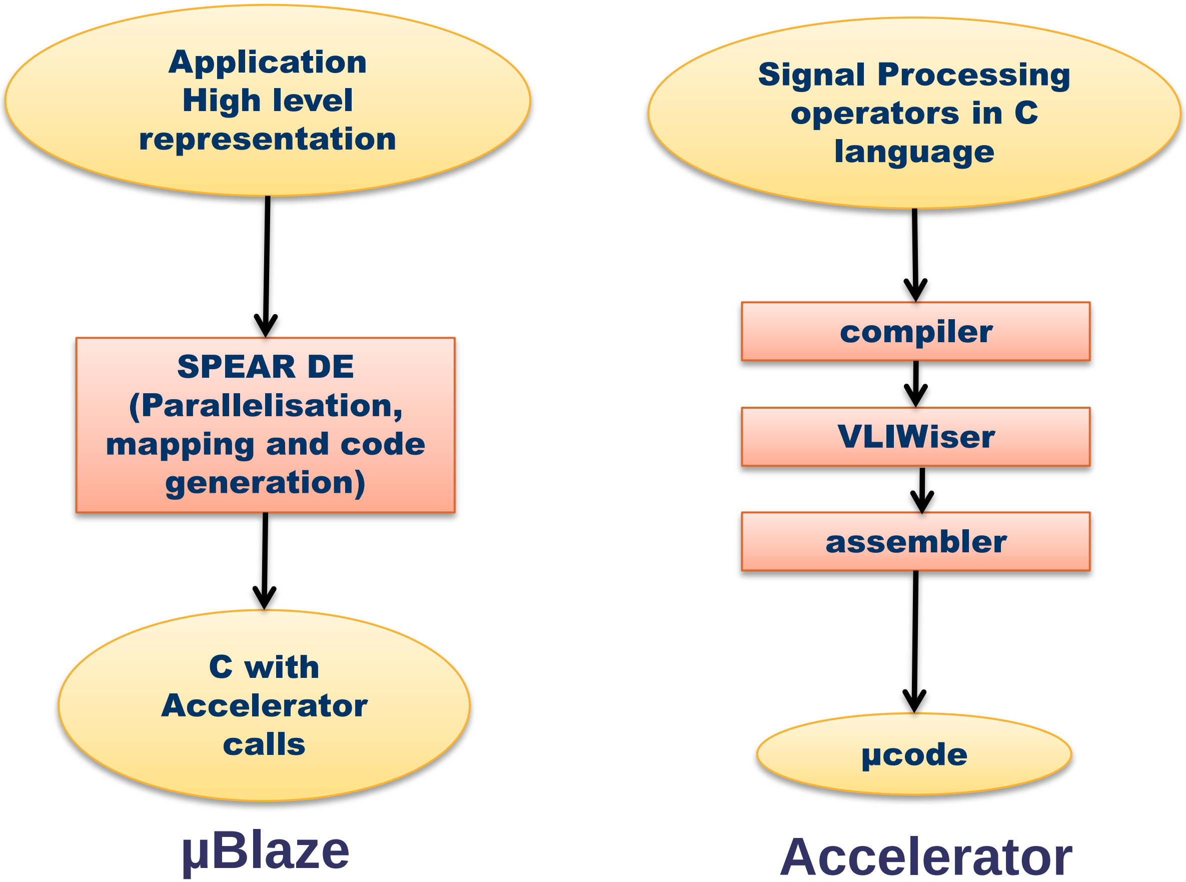
Xilinx Virtex-6 SX315
Consumption : ~50W

PE of TeraTS

The PE is a 32 bits processor

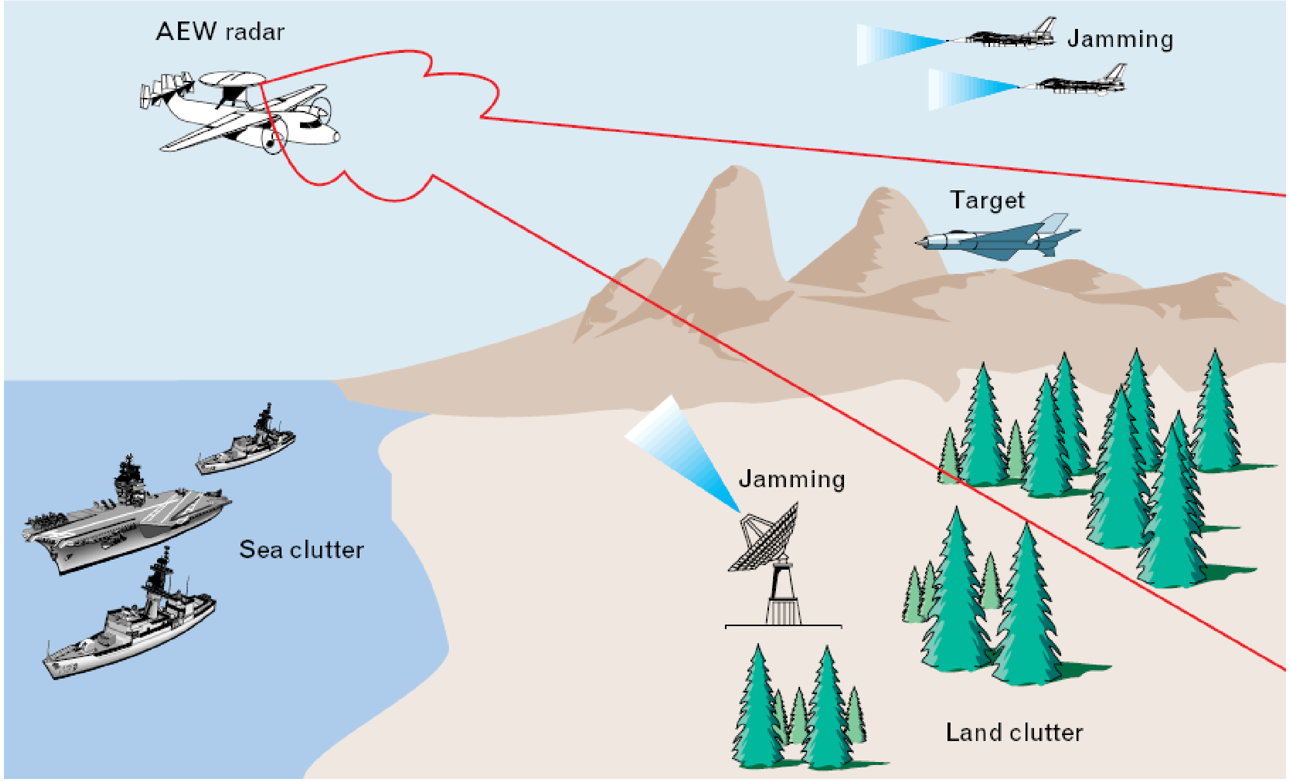


TeraTS Programming tools



Application development impacts

Objectives: remove clutter (ground reflexion) and detect moving targets.



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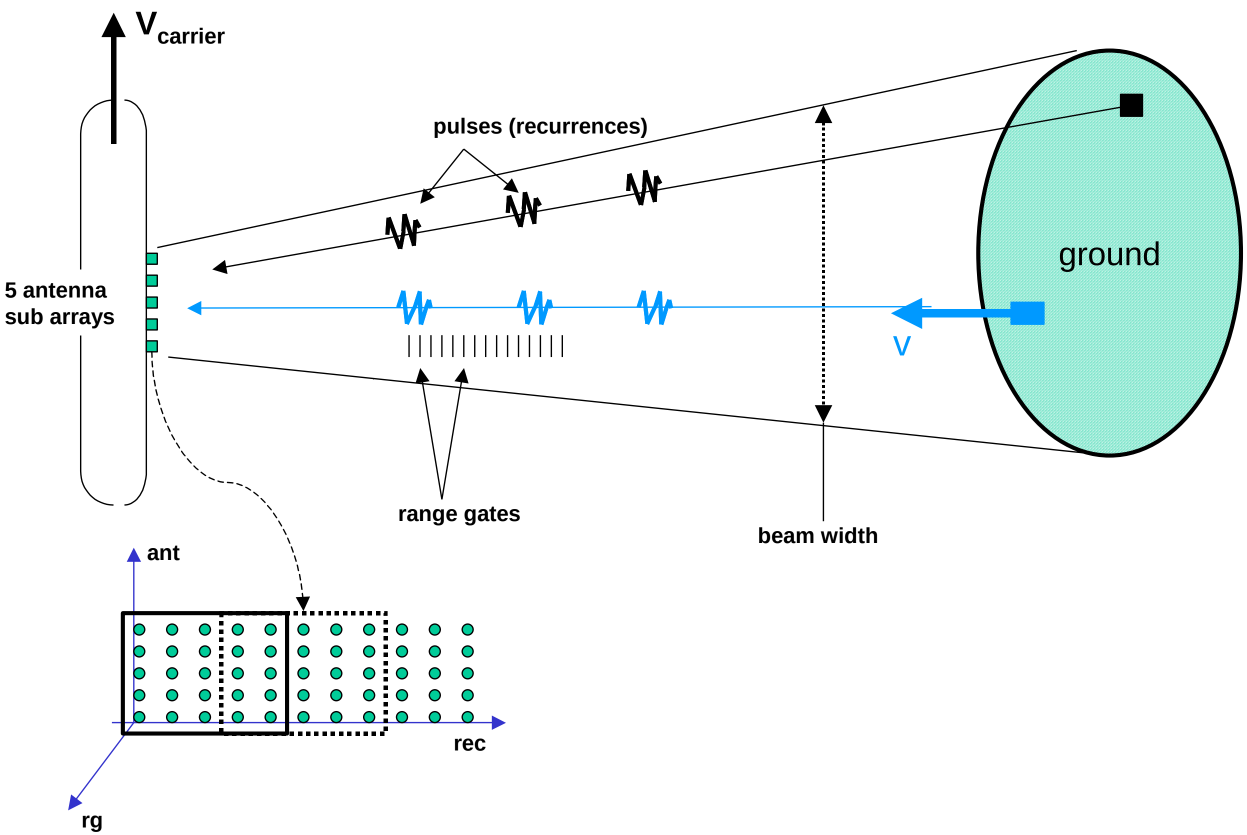
STAP principles



Surveillance of the *ground* by *air:* Detection of Moving Targets STAP computes dynamically the best filter to suppress the clutter (ground reflexion) and detect the moving targets

•An aircraft illuminates the ground, with a beam orthogonal to its velocity, by sending repeatedly sequences of periodic pulses (denoted rec)
•The echoed signal is received on 5 sensors (ant)
•The received signal is sampling at a given frequency, each sample corresponding to a distance called a range gates (rg) (typically 15 meters for a 10 MHz sampling)

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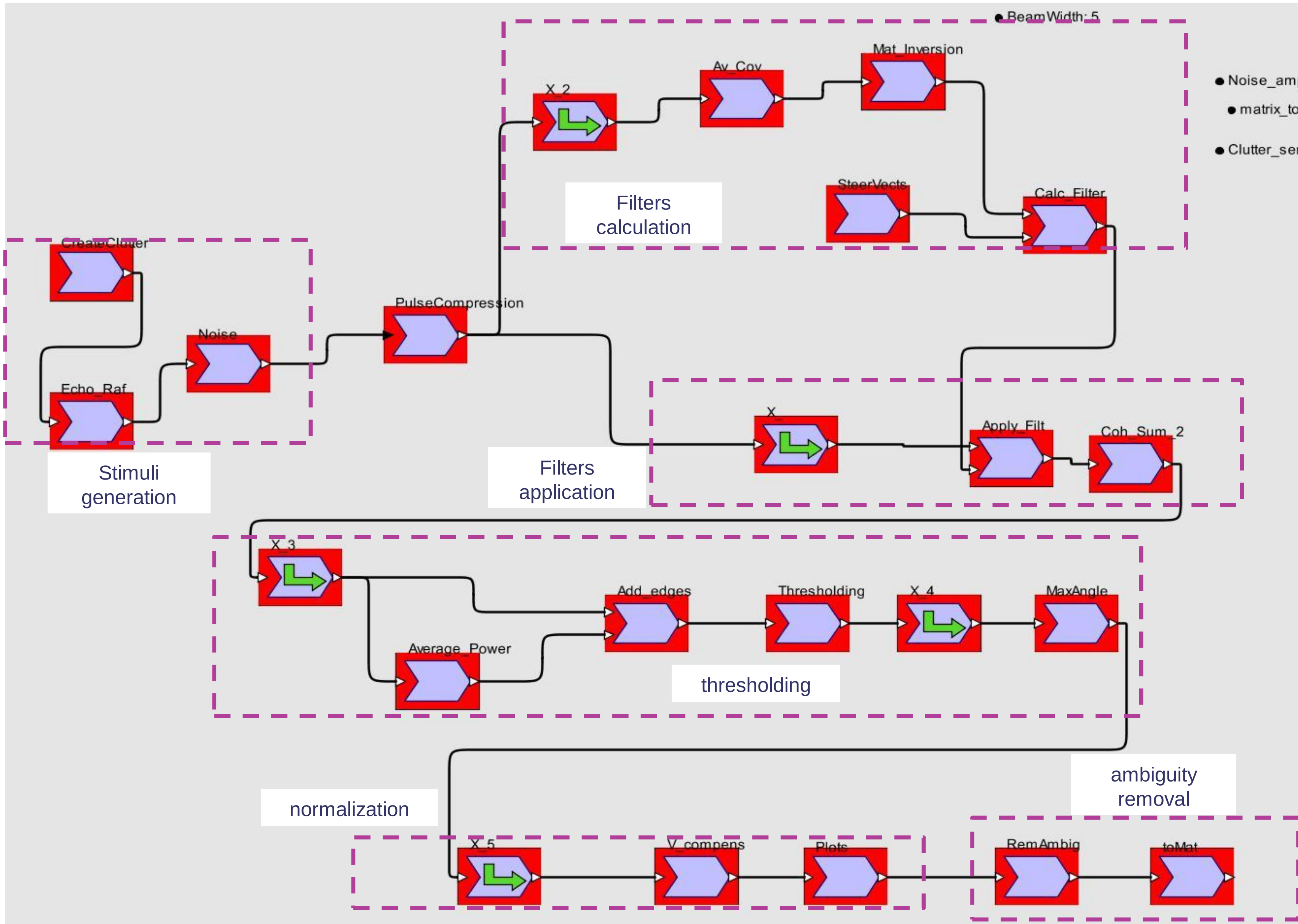
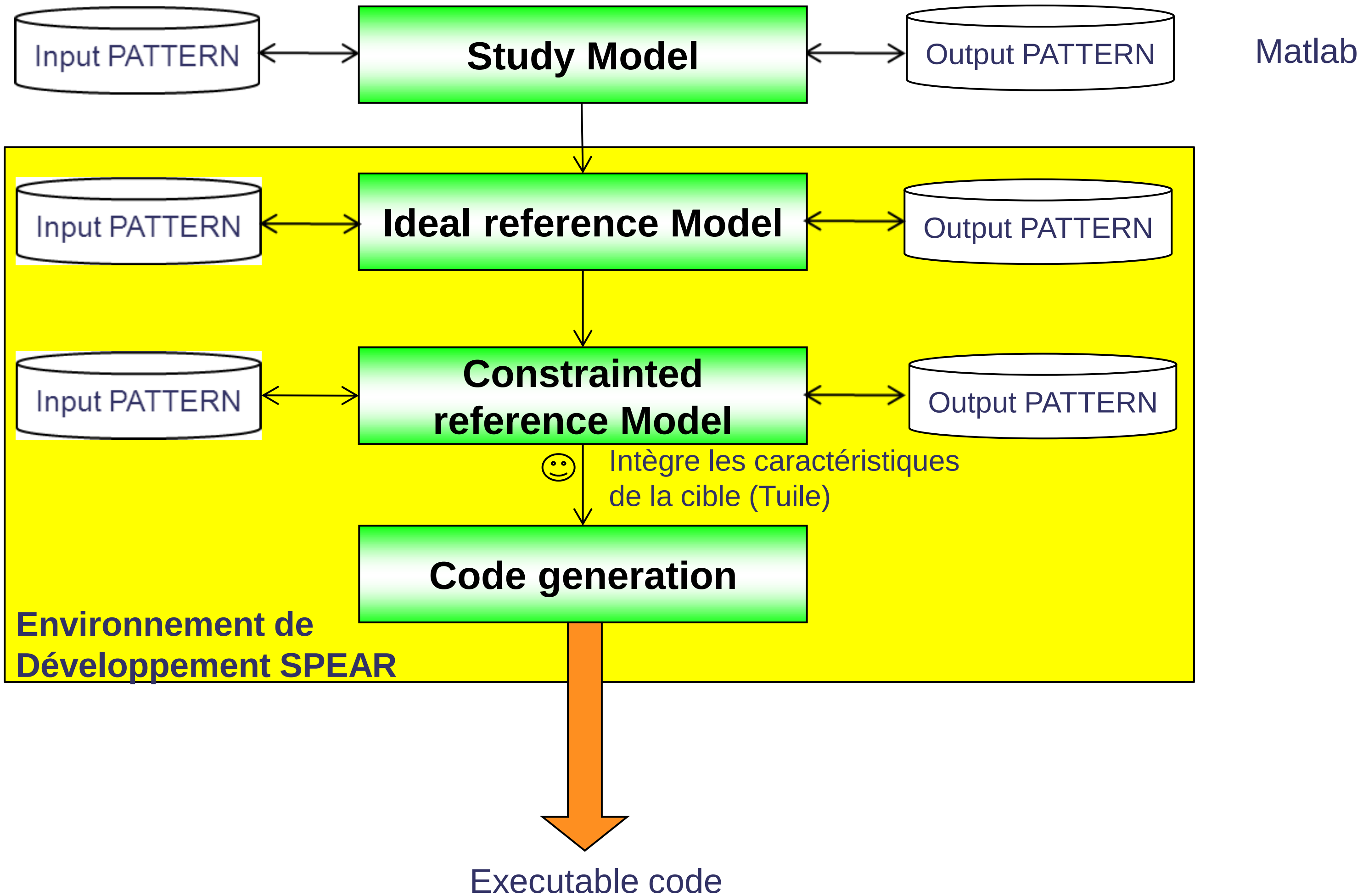
STAP algorithm



Programming flow



Constrainted reference model

- **Fixed-point arithmetic compliant with the constraints of the target:**
  - Multiplication, addition : 32 bits
  - Accumulation: 70 bits
  - Barrel shifter
- **Signal noise ratio**
- **No overflow**

This conversion can be very long.

It requests communication between engineers who don't speak the same language:

Algorithm -> software -> hardware

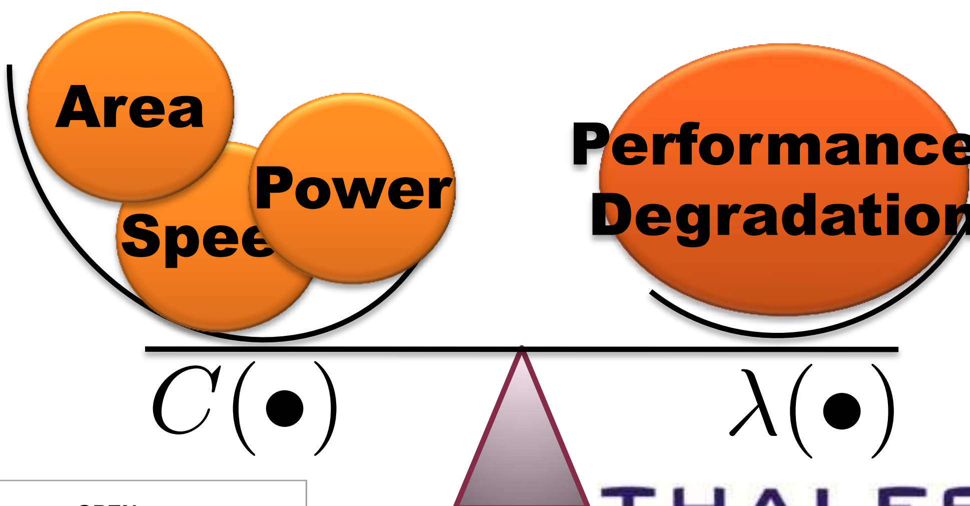
Fixed-Point Conversion

Loss of precision incurs loss of performance

Essentially, an optimization process

- Find trade-off between accuracy and cost
- Determine the number of bits for each data

- Manual conversion is tedious
- Strong need of tools



Current Limit of Commercial tools

Accuracy evaluation is performed using bit-true simulations

- **Fixed-point simulation is very long**
- **Word-length optimisation time is prohibitive**
- **Used in all existing tools**
  - HDL coder Matlab (Mathworks), Vivado (Xilinx), Catalytic (Mentor Graphics)

Strongly user-guided iterative process with long simulations in the loop

It is the reason why we are involved in DEFIS project (ANR)

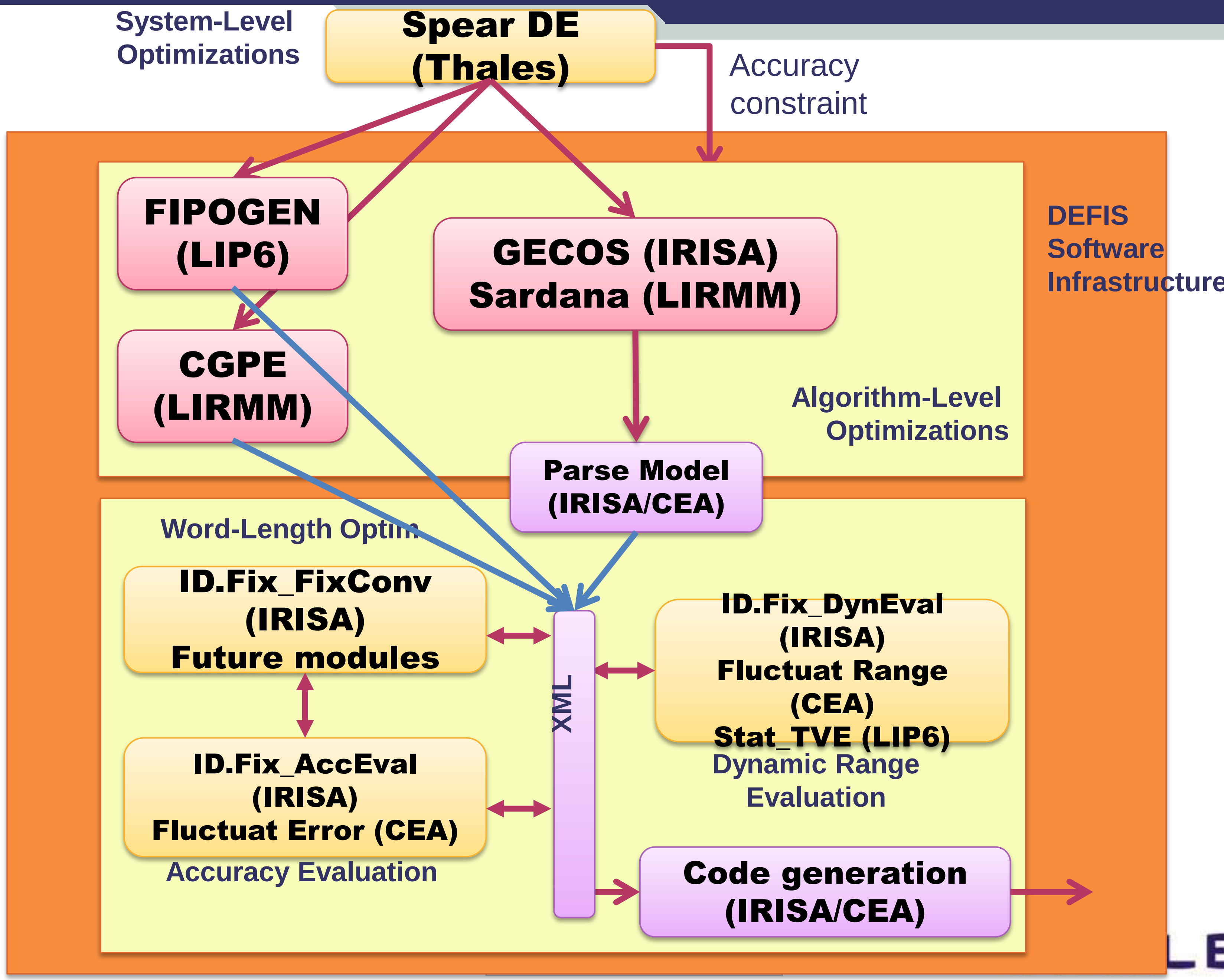
Aim of the DEFIS project is threefold

- To provide **new methods** for fixed-point conversion
  - Analytical and efficient simulation-based methods
- To develop a **complete software infrastructure** for automatic fixed-point conversion
- To demonstrate the quality of DEFIS flow on two **industrial applications**

DEFIS at a glance

- Nov. 2011 to Feb. 2015 (40 months), today ≈ T0+19
- Pôle Images & seaux, Pôle System@tic
- 2 PhD grants, 1 Engineer/PostDoc (36 months)
- 994.500€, 281 person.months

Software Integration



Perspectives

Insertion in the development flow

Reduction of the development cost

Avoid risks when using dedicated accelerators based on fixed-point ALU

Thank you for your attention !

Questions

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